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Substitute for form 1449/PTO

JUN 04 2004

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number 10/790,336
Filing Date 03/01/2004
First Named Inventor Brunette et al
Art Unit
Examiner Name
Attorney Docket Number 136P26US01

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
JS		US- 5,522,132	06-04-1996	Mattei	
JS		US- 5,920,242	07-06-1999	Oya et al	
JS		US- 6,031,188	02-29-2000	Pluymers et al	
JS		US- 6,172,305	01-09-2001	Tanahashi	
JS		US- 6,184,477	02-06-2001	Tanahashi	
JS		US- 6,329,604	12-11-2001	Koya	
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JS		US- 6,388,206	05-14-2002	Dove et al	
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		US-			
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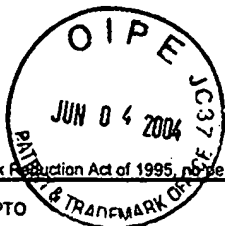
FOREIGN PATENT DOCUMENTS					
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Examiner Signature	Date Considered
<i>[Signature]</i>	7/8/05

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PTO/SB/088 (08-03)

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JS		SARFARAZ et al; Interconnect Characterization...Digital Applications; (rambus.com); IEEE 9th Topical Meeting Electrical Performance; Oct23-25, 2000pp1-4; Mountain View, CA, US	
JS		CHEN et al; Via and Return Path Discontinuity Impact on High Speed Digital Signal Quality; EPEP Conf. www.sigrity.com; Oct 2000; pp1-4	
JS		ULTRACAD DESIGN INC.; The Effects of Vias on PCB Traces; ultracad.com; 1994; pp1-6; Bellevue, WA, US	
JS		COHEN, TOM; Practical Guidelines for the implementation of Back Drilling Plated Through Hole Vias in Multi-gigabit Board Applications; DesignCon 2003; pp1-10; Nashua, NH, US	
JS		ZEGARAC, Zoran; Signal Integrity issues of dense pin field and via interconnections; pp1-4; University of Western Australia No Date cannot consider	
JS		COHEN et al; Signal Integrity Considerations for High Speed Data Transmission in a Printed Circuit Board System; IMAPS 1998; www.teradyne.com; pp1-6	
JS		TALLO, Joseph; Designing an X-Band T/R Module Package; Kyocera; Ansoft 2003 HFSS Users Workshop; www.ansoft.com; pp1-32	

Examiner Signature

Date

Considered

7/8/05

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